Experimental comparison between Fully and Partially depleted SOI MOSFETs through analog parameters

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***Abstract*—This work presents the analog behavior comparison between fully and partially depleted SOI transistors. The devices are set to operate in the saturation region, and analog parameters like transconductance (gm_{sat}), output conductance (g_D), transistor efficiency (gm/Id), Early voltage (V_A) and intrinsic voltage gain (A_V) were analyzed. Fully depleted devices presented better analog characteristics due to the better electrostatic coupling between gate and channel and due to the kink effect suppression.**

Keywords—SOI MOSFETs, experimental, analog, transistors

I. Introduction

Digital integrated circuit (IC) development has been driving the semiconductor industry for years, following higher-performance demands and new processor centered applications. However, new market trends and requirements have been shifting the course of microelectronics lately towards Mixed-Signal IC development focusing on analog expertise.

The Metal-Oxide-Semiconductor Field Effect transistor, in its most used technology (CMOS), had a fundamental role in the ICs industry since it´s invention, due to its excellent characteristics in digital applications, high scalability, easy fabrication processes, among others [1]. However, the Silicon-On-Insulator (SOI) MOSFET technology, considered an evolution of the CMOS, has been more attractive to some applications, presenting many solutions to problems that CMOS has been suffering, due to higher scalability and better control of Short Channel Effects [2], for example, and still being cheaper than the newest 3D solutions, such as the Fin-FETs.

So, the MOSFET devices have been the key to the traditional approach in ICs industry for decades, where the focus were on digital appliances and processing, and support it, when needed, with analog submodules. This resulted in "Small-A Big-D" devices, which follows thoroughly the Moore's Law: highest-performance computing on cutting-edge process nodes, low cost-per-function and high production volume.

Nowadays, the most discussed topic, specially inside the semiconductor environment, differs a bit. Internet of Things (IoT) is the next big wave that will drive the Semiconductor Industry to the next level. IoTs edge nodes invariably will consist of "Big-A Small-D" devices [3].

That is why it becomes so important to study and understand how the SOI (130 nm and smaller) could bring benefits and improvements to new devices and applications that are emerging every day with the IoT expansion, in terms of performance, stability and power consumption. The fully depleted (FD) SOI is one of devices that could substitute the CMOS technology on ICs for IoT applications, and in this work, it is compared with partially depleted (PD) SOI transistors. For a better comparison, both types of devices are of the 130 nm technology node [3].

II. Experimental Details

The studied devices were fabricated at imec on (100) SOI substrate with the following characteristics: the gate and buried oxide thicknesses (t_{OXF} and t_{OXB}) are 2.5 nm and 390 nm, respectively. For partially depleted devices, the silicon film (t_{Si}) is 100nm and the channel doping concentration (Na) is $5.5x10^{17}cm^{-3}$, while for fully depleted one t_{Si} is 30nm and Na is $1x10^{18}$ cm^{-3}. For both PD and FD devices, the channel length varies from 1µm down to 300 nm. More details can be found in [4].

The devices were mesured with drain voltage (V_D) equal to 800 mV for the FD devices, and 700 mV and 800 mV for the PDs, and the gate voltage (V_{GS}) from 0 to 1.25 V. The substrate was grounded for all measurements. All the measures were made respecting the saturation condition [5], shown in (1).

$$V_D \geq V_{GS} - V_{TH} \quad (1)$$

III. Results and Discussion

Figure 1 shows the output characteristics for PD and FD SOI MOSFETs for long and short channel devices and for overdrive voltage ($V_{GT}=V_{GS}-V_t$) of 200 mV. From Figure 1, one can observe that FD devices have the better plateau in the saturation region mainly for longer channel devices. When it is compared with PD devices behavior, it is noted an abrupt elevation of the current level for drain voltages higher than 700 mV. This behavior is called Kink Effect and it is only present on PD SOI transistors.

Figure 2 presents the normalized transconductance on saturation for channel lengths varying from 1000 nm down to 300 nm for FD and and down to 500 nm for PD devices. This parameter indicates the capacity to control the drain current of the transistor (I_D), through the applied gate voltage (V_G), i.e., how well it controls the charges in the active region of the device, the channel region [6]. This parameter has a strong inverse relation with the channel length, given by (2).

$$gm_{sat} = \mu . N . C_{OX} . \frac{W}{L} (V_{GS} - V_T) \quad (2)$$

Where C_{OX} is the gate oxide capacitance, μ is the effective carriers mobility and N is the body factor constant.

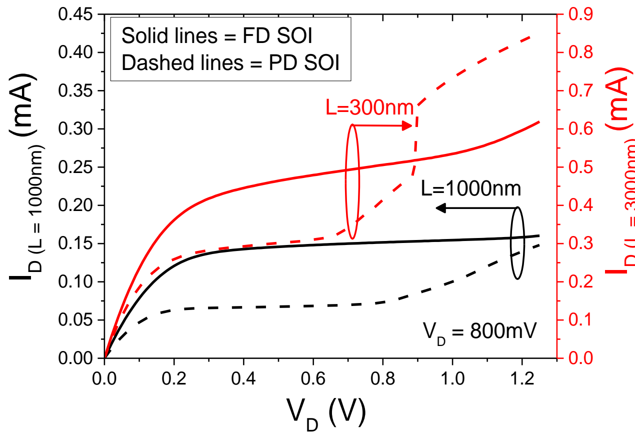

Fig. 1. Drain current as a function of drain voltage for FD and PD SOI devices for two different channel lengths.

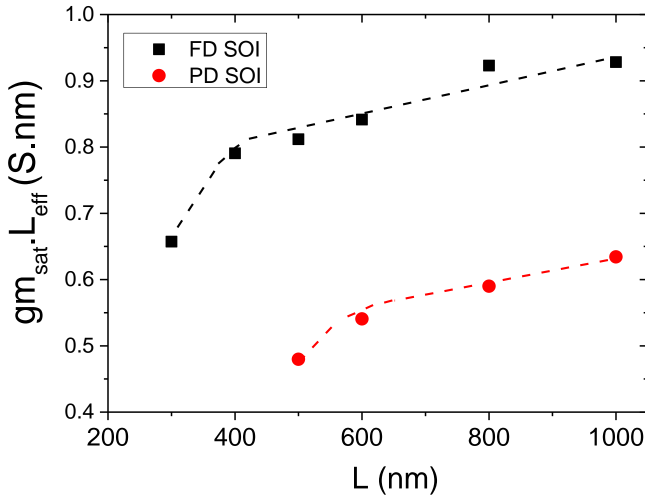

Fig. 2. Normalized transconductance as a function of channel length for PD and FD SOI transistors.

Thus, to eliminate this dimension influence on gm_{sat}, this parameter needs to be normalized. The normalization is done by multiplying the values of each transconductance by the effective channel length value (L_{eff}) of each device, thus eliminating the strong relation with L.

From Figure 2, it is noted that the obtained values of transconductance for FD devices are higher than in PD devices. This can be explained by the greater coupling between gate and channel in FD devices, which is due to the smaller t_{si}, and also, by greater effective mobility [1,2].

It is also observed that, in the FD transistors, there is an abrupt drop in transconductance only in very short channels (300 nm). In PDs, the drop occurs for transistors with larger channels (L < 600 nm), which indicates that the fully depleted devices have greater control over the channel charges, becoming more immune to short channel effects (SCE) [6].

The output conductance (g_D) is a parameter based on output current and voltage. It indicates how much the drain voltage has influence over the charges inside the device channel [6,7]. It is given by Equation 3

$$g_D = \frac{\Delta I_D}{\Delta V_D} \approx \frac{I_D}{V_A} \quad (3)$$

It is possible to do this approximation when the saturation voltage of the device is small and negligible near the Early voltage (V_A). The output voltage difference is actually given by the sum of the Early voltage, which is the voltage of interest to qualify the amplification of the device, discussed later, with the voltage V_{Dsat} (voltage to be applied to the drain of the device so that it is operating in the saturation region) [7]. The non-simplified formula is given by Equation 4.

$$g_D = \frac{\Delta I_D}{V_A + V_{Dsat}} \quad (4)$$

The output conductance values (g_D) should be as low as possible, since it is not desirable for this drain voltage to exert any kind of control over the current of the transistor.

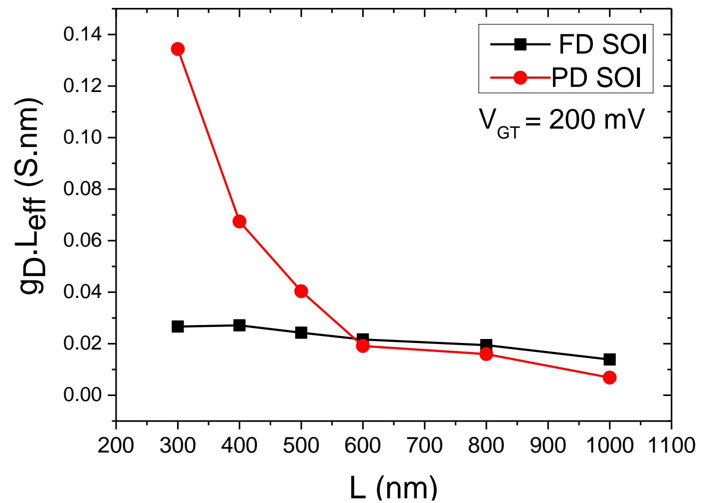

Fig. 3. Normalized output conductance as a function of channel length for PD and FD SOI transistors.

This parameter is closely linked to the intrinsic voltage gain of the device, another extremely important parameter to be studied for analog applications. The output conductance was also normalized, so that a more detailed analysis could be performed.

Figure 3 shows that, for a gate voltage overdrive of 200 mV ($V_{GT} = V_G - V_T$), the influence of the drain voltage is higher on shorter channels of both types of devices. This occurs because, in smaller channels, the region of the channel under the control of the drain electric field is proportionally larger when compared to the total length of the channel. In longer channel devices, this region controlled by the drain is negligible, since most of the charges are still being controlled by the transistor gate.

This influence, however, is much stronger in PD devices with channel lenghts smaller than 600 nm. The g_D is about five times larger in the shortest channel as compared to the same channel FD transistor. This difference is due to the smaller t_{Si} of the FD devices, which prevents that the drain control region extends to a channel region as in PD one [6,7].

It is known that the maximum value of transistor efficiency (gm/I_D) occurs in weak inversion and it is inversely proportional to the Subthreshold Slope (SS). Due to a lower body factor (n), FDs have significantly higher gm/I_D values than PD and Bulk MOSFETs, which are: FD = 35 V^{-1} and PD and Bulk = 25 to 30 V^{-1} [6].

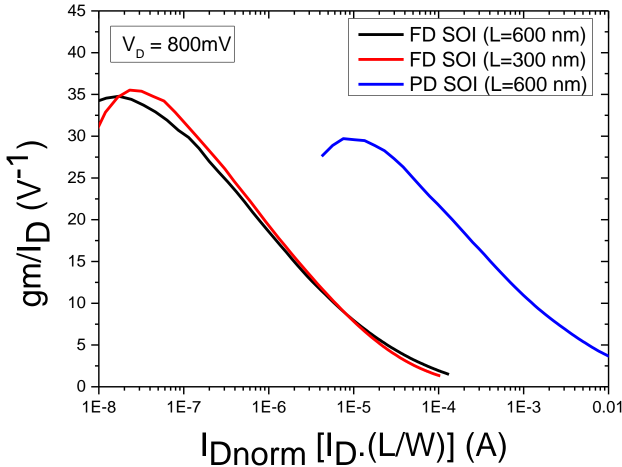

Fig. 4. Transistor efficiency as a function of normalized drain current

From figure 4, it was not possible to observe the gm/I_D characteristic for 300 nm channel length of the PD device because the device had a strong short channel effect.

The Early voltage (V_A) is extracted from the linear extrapolation of the plateau of output curve (saturation region). It is desirable that this parameter assumes very large values (in module), since it is directly proportional to the intrinsic gain of the transistor [6].

In this work, the extrapolation was done for two different V_{DS} ranges (0.65 to 0.75 V and 0.7 to 0.9 V) for both types of devices, in order to better understand why the kink effect affect the V_A.

From Figure 5, a reduction of V_A with the reduction of channel length is observed for both devices, as expected. When comparing both types of devices in the same V_{DS} range (0.65 to 0.75 V), a better performance of the FD in shorter channels is observed, which will result in a higher gain in relation to the PD[7] due to the better gate control over the channel charges.

When considering another operating range (0.7 to 0.9 V), it is important to remind that besides the better charge control, for PD transistors, it is also necessary to take into account the Kink Effect, which abruptly increases the current levels resulting in a higher slope and consequently even lower V_A values (almost zero). This makes this voltage range impractical for these PD devices.

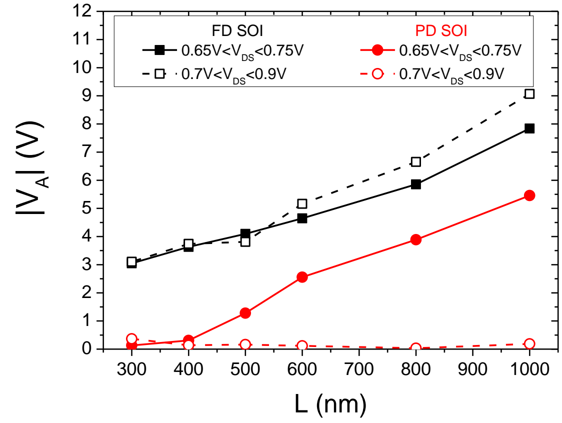

Fig. 5. Early Voltage transconductance as a function of channel length for PD and FD transistors

The intrinsic voltage gain of a transistor can be calculated by gm/I_D ratio multiplied by Early voltage (Equation 5) or by the transconductance over output conductance .

$$A_V = g_m \times \frac{V_A}{I_D} = \frac{g_m}{g_D} \quad (5)$$

Figure 6 shows the intrinsic voltage gain values of the studied SOI transistors, as a function of the channel length. The A_V values were extracted mathematically using the experimental values of transconductance in saturation and output conductance.

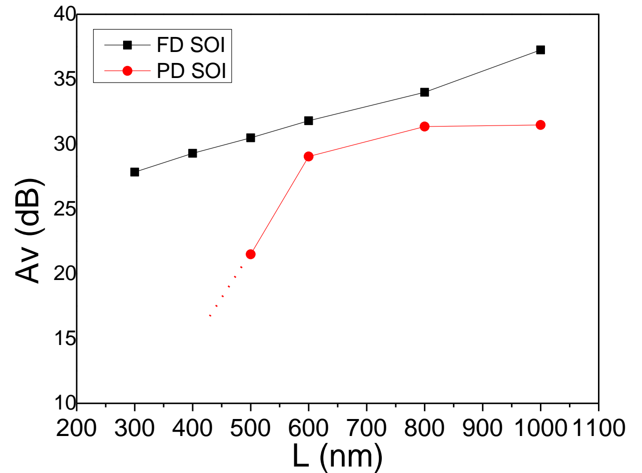

Fig. 6. Intrinsic Voltage Gain transconductance as a function of channel length for PD and FD transistors

A significant A_V reduction is observed as the channel length is reduced. This reduction can be understood by the higher total number of charges that is controlled by drain bias that results in higher output conductance [6] and smaller transconductance values. The second explanation would be due to the reduction of the Early Voltage, that is a consequence of higher g_D .

Comparing the two devices, the gain values in PD suffer a much more significant reduction.

IV. Conclusions

In this paper, FD and PD SOI devices were analyzed under the analog point of view, using experimental data.

Through the normalized transconductance, it was verified that FD devices presents a better SCE control, in comparison with the PD one, due to the thinner t_{si}, providing a better coupling between the gate and the channel.

The output conductance shows that, for long channel lengths, the control exercised by the drain voltage is almost the same in both devices, but it can increase significantly in PDs, due to a wider t_{si}, allowing the depletion regions to extend to a greater area in the active region of the transistor.

Aiming to analyze the potential of SOI transistors for analog application, the Early voltage and the intrinsic voltage gain were extracted. Through the V_A, it was possible to note the importance of the choice of the amplification region in PD devices, to guarantee that this region is not comprehending the Kink Effect, which could compromise the gain of the device. Higher Early voltages, and consequently higher intrinsic voltage gains, were obtained for fully depleted devices with long channel lengths. Therefore, these results shows the greater analog performance to FD SOI when compared with PD ones.

Considering all the obtained results, the FD SOI transistors showed to be the best candidate for the ICs analog industry, contributing to its adoption expansion in the applications of IoT, sensors, dedicate ICs, and others.

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